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Propagation Mechanism and Suppression Strategy of DC Faults in AC/DC Hybrid Microgrid

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Abstract: Due to their efficient renewable energy consumption performance, AC/DC hybrid microgrids have become an important development form for future power grids. However, the fault response will be more complex due to the interconnected structure of AC/DC hybrid microgrids, which may have a serious influence on the safe operation of the system. Based on an AC/DC hybrid microgrid with an integrated bidirectional power converter, research on the interaction impact of faults was carried out with the purpose of enhancing the safe operation capability of the microgrid. The typical fault types of the DC sub-grid were selected to analyze the transient processes of fault circuits. Then, AC current expressions under the consideration of system interconnection structure were derived and, on this basis, we obtained the response results of non-fault subnets under the fault process, in order to reveal the mechanism of DC fault propagation. Subsequently, a current limitation control strategy based on virtual impedance control is proposed to address the rapid increase in the DC fault current. On the basis of constant DC voltage control in AC/DC hybrid microgrids, a virtual impedance control link was added. The proposed control strategy only needs to activate the control based on the change rate of the DC current, without additional fault detection systems. During normal operations, virtual impedance has a relatively small impact on the steady-state characteristics of the system. In the case of a fault, the virtual impedance resistance value is automatically adjusted to limit the change rate and amplitude of the fault current. Finally, a DC fault model of the AC/DC hybrid microgrid was built on the RTDS platform. The simulation and experimental results show that the control strategy proposed in this paper can reduce the instantaneous change rate of the fault state current from 19.1 kA/s to 2.73 kA/s, and the error between the calculated results of equivalent modeling and simulation results was within 5%. The obtained results verify the accuracy of the mathematical equivalent model and the effectiveness of the proposed current limitation control strategy.

Keywords: AC/DC hybrid microgrid; bidirectional power converter; current limiting strategy; fault propagation; mechanism analysis

Citation: Xiao, C.; Ren, Y.; Cao, Q.; Cheng, R.; Wang, L. Propagation Mechanism and Suppression Strategy of DC Faults in AC/DC Hybrid Microgrid. *Processes* **2024**, *12*, 1013. https://doi.org/10.3390/pr12051013

Received: 28 March 2024
Revised: 13 May 2024
Accepted: 15 May 2024
Published: 16 May 2024

1. Introduction

Hybrid AC/DC microgrid systems play a crucial role in the modernization of power systems due to their ability to integrate renewable energy sources, improve system efficiency, and enhance grid resilience [1–3]. The combination of AC and DC components in a hybrid microgrid allows for increased flexibility, reliability, and controllability, making it a promising solution for meeting the growing energy demands of modern society [4].

The occurrence of DC grounding faults [5] in hybrid AC/DC microgrid systems can pose serious safety hazards and system instability. Factors such as multiple grounding points, high DC system impedance, and a lack of fault-current-limiting devices contribute

to the propagation of DC faults, leading to voltage fluctuations, equipment damage, and potential system-wide disruptions. Understanding the mechanisms of DC fault propagation in hybrid microgrids is essential for developing effective mitigation strategies to ensure the reliable operation of these systems.

Research on the propagation mechanisms of DC grounding faults in hybrid microgrid systems is currently focused on investigating the impacts of fault types, fault locations, system parameters, and grounding configurations on fault propagation behaviors [6–8]. By studying these factors, researchers aim to gain insights into the mechanisms that govern fault propagation in hybrid microgrids and develop strategies to mitigate their effects. Advanced modeling and simulation techniques have been employed to analyze fault propagation dynamics and assess the effectiveness of different fault detection and isolation methods [9–11].

Research on the characteristics of DC faults is mostly conducted in the context of voltage-sourced converter high-voltage direct current (VSC-HVDC) systems [12,13], including the proposal of control strategies and relay protection measures for commutation failure issues. However, system modeling and mechanism analysis under commutation failure conditions require further study. Typical DC fault characteristics include a sharp increase in short-circuit current, necessitating not only consideration of current limiting measures for DC lines but also addressing the impacts of DC faults on power converters and AC equipment. One study [14] has analyzed the transient processes of pole-to-pole short circuits and single-pole grounding faults in DC cable lines and proposed methods for locating grounding faults, while others [15–17] presented models for calculating the short-circuit current between poles in DC distribution networks but did not consider the impact of DC faults on AC lines and converters. In [18], the diodes inside the converter were replaced with controllable electronic tubes, thus achieving isolation of DC faults using the converter, but at the cost of high investment and increased control complexity.

In the current research landscape, various approaches are being explored to suppress fault currents in DC sub-grids within hybrid microgrid systems. Fault current limiters (FCLs) are one of the primary methods used to limit fault currents and prevent damage to system components [19–24]. Different types of FCLs, such as superconducting FCLs, resistive FCLs, and hybrid FCLs, are being studied for their effectiveness in reducing fault currents during fault events. Additionally, active fault current limiting techniques, including current control strategies and power electronics-based solutions, are being developed to actively control fault currents and enhance system protection.

Furthermore, researchers are investigating fault current mitigation strategies that involve the coordination of protective devices [25–28], such as circuit breakers and fault detection systems, to improve the speed and accuracy of fault detection and isolation in DC sub-grid systems. Through integrating intelligent protection schemes and communication technologies, researchers aim to enhance the reliability and safety of hybrid AC/DC microgrid systems by effectively suppressing fault currents and minimizing the impact of DC grounding faults. However, the fault current limitation control strategies mentioned in the above studies require additional detection or control devices, which increases the associated investment and maintenance costs and makes the system more complex.

Based on an AC/DC hybrid microgrid with an integrated bidirectional power converter, research on the interaction impacts caused by DC faults were carried out with the purpose of enhancing the safe operation capability of microgrids. The typical fault types of the DC sub-grid were selected, in order to analyze the transient process of fault circuits. Then, AC current expressions under the consideration of system interconnection structure were derived and, on this basis, we obtained the response results of non-fault subnets in fault process, in order to reveal the mechanisms of DC fault propagation. Subsequently, a current limitation control strategy based on virtual impedance control is proposed to address the rapid increase in the DC fault current. On the basis of constant DC voltage control in AC/DC hybrid microgrids, a virtual impedance control link is added. The proposed control strategy only needs to activate the control based on the change rate of the

DC current, without additional fault detection systems. During normal operations, virtual impedance has a relatively small impact on the steady-state characteristics of the system. In the case of a fault, the virtual impedance resistance value is automatically adjusted to limit the change rate and amplitude of the fault current.

The remainder of this paper is organized as follows. Section 2 presents the analysis of the fault propagation mechanism in the DC sub-grid. Section 3 provides the current limitation control strategy for DC fault currents. The simulation results are discussed in Section 4. Conclusions are drawn in Section 5.

2. Analysis of Fault Propagation Mechanism in DC Sub-Grid

The main circuit structure of the AC/DC hybrid microgrid is shown in Figure 1. The typical fault types of the DC sub-grid include inter-pole, short-circuit fault and single-pole ground fault. The fault current on the DC sub-grid will rapidly increase until it reaches a large value, due to the smaller equivalent impedance. To avoid burning out the insulated gate bipolar transistor (IGBT) of the bidirectional power converter (BPC), the IGBT can be immediately turned off at the moment of fault due to its self-protection function. However, the AC sub-grid will supply a short-circuit current through freewheeling diodes, which will not be able to isolate DC faults, thus affecting the safe and stable operation of the entire system.

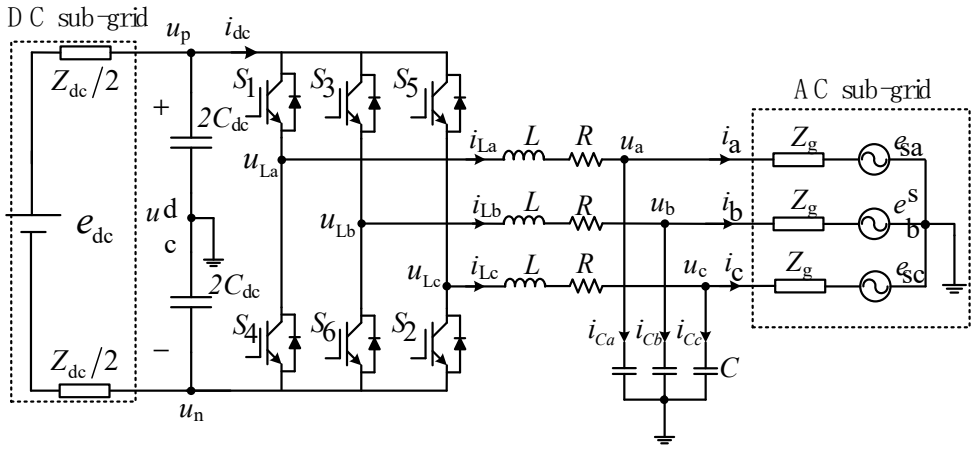

Figure 1. Main circuit structure of AC-DC hybrid microgrid.

2.1. Response Characteristics of AC Sub-Grid in Case of Inter-Pole, Short-Circuit Fault in DC Sub-Grid

A schematic diagram of the inter-pole, short-circuit fault is shown in Figure 2. During the initial discharge stage of the fault, the DC capacitor voltage U_{dc} is greater than the AC voltage. The BPC is equivalent to a second-order RLC discharge circuit, as shown in Figure 2.

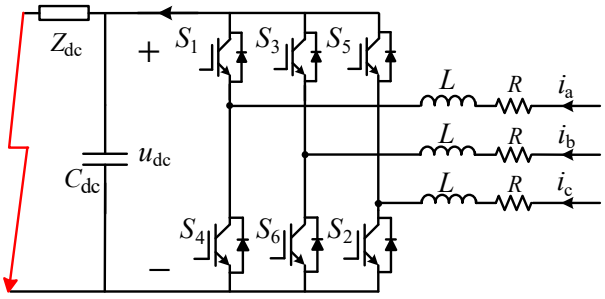

Figure 2. Inter-pole, short-circuit fault of DC sub-grid.

The equivalent damping of the DC sub-grid satisfies the condition of $R_{dc} < 2\sqrt{L_{dc}/C_{dc}}$. The capacitor voltage decays and oscillates to zero in an underdamping state. When U_{dc} is below the AC voltage, it enters the AC feeding stage. At this time, the diode follows the natural commutation principle of uncontrolled rectification. The AC power supply and DC capacitor discharge to the fault point simultaneously, as shown in Figure 3. In the figure, the red line represents the current flow paths.

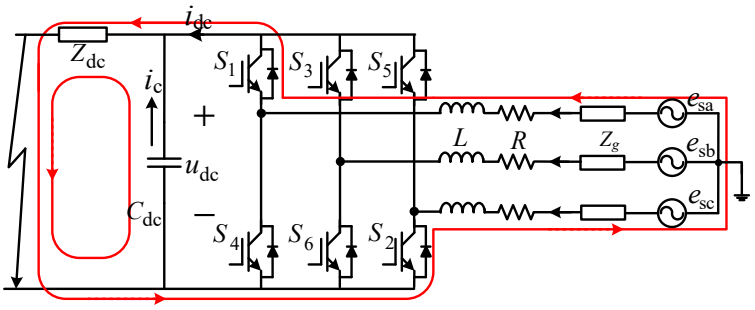

Figure 3. Short-circuit current path in AC feed stage.

When the DC voltage decays and oscillates to zero, the diode conducts simultaneously. The opposing electromotive force of the short-circuit reactance in the DC sub-grid causes all diodes of the BPC to conduct simultaneously, which reduced the DC voltage to zero. The DC sub-grid forms a first-order discharge circuit and, due to the conduction of all freewheeling diodes, the AC sub-grid is equivalent to a three-phase, short-circuit fault, as shown in Figure 4.

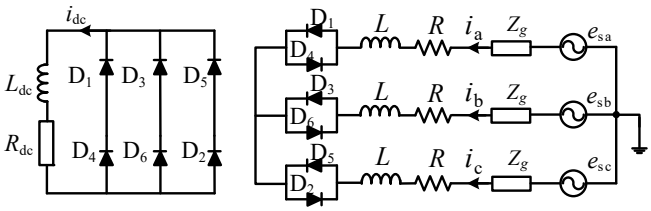

Figure 4. Equivalent diagram of all diodes conducting.

Taking the transient response of the short-circuit current in phase A of the AC sub-grid during an inter-pole, short-circuit fault as an example, assuming that the voltage source crosses zero at $t = 0$, the voltage in phase A is $e_{sa} = E_{sa} \sin \omega t$, $I_{m|0|}$ is the instantaneous current value of phase A, and I_{dc} is the instantaneous value of the DC short-circuit current. The current of phase A can be expressed as

$$i_a = I_m \sin(\omega t - \varphi) + \left[I_{m|0|} - I_m \sin(-\varphi) \right] e^{-\frac{t(R+R_g)}{L+L_g}} \quad (1)$$

where i_{dc} is current of phase A, $I_m = E_{sa} / \sqrt{(R+R_g)^2 + \omega^2 (L+L_g)^2}$ is voltage amplitude of phase A, L is the filter inductance of the converter, R is the parasitic resistance of filter inductance, R_g is equivalent resistance of AC power supply, and L_g is equivalent inductance of AC power supply. The DC current i_{dc} can be expressed as

$$i_{dc} = I_{dc} e^{-\frac{L_{dc}}{R_{dc}} t} \quad (2)$$

where i_{dc} is the current amplitude of phase A, L_{dc} is DC inductance, and R_{dc} is DC resistance.

According to Equation (1), during the simultaneous conduction of diodes, the AC short-circuit current consists of periodic and non-periodic components, and the DC short-circuit current decays with time. Then, the system operates in steady state and the AC short-circuit current of each phase shows sinusoidal variation with equal amplitude and

a phase angle difference of 120°, due to the symmetry of the three-phase circuit. The magnitude of the short-circuit current depends on the voltage amplitude of the AC power supply and the total impedance of the AC/DC sub-grid short-circuit circuit.

2.2. Response Characteristics of AC Sub-Grid in Case of Single-Pole Ground Fault in DC Sub-Grid

The single-pole ground fault of the DC sub-grid is shown in Figure 5. During the initial capacitor discharge stage of the single-pole ground fault, the positive voltage u_p of the DC sub-grid is greater than the AC phase voltage, and the BPC is equivalent to a RLC discharge circuit. When u_p decays below the AC phase voltage, the system operates in AC feedback mode, as shown in Figure 6. The AC sub-grid will still offer the power supply to the DC sub-grid, due to the normal operation of the AC sub-grid. When the positive electrode potential remains at zero due to grounding, the negative electrode potential u_n changes from $-0.5u_{dc}$ to $-u_{dc}$, and the potential difference between the positive and negative poles remains at u_{dc}.

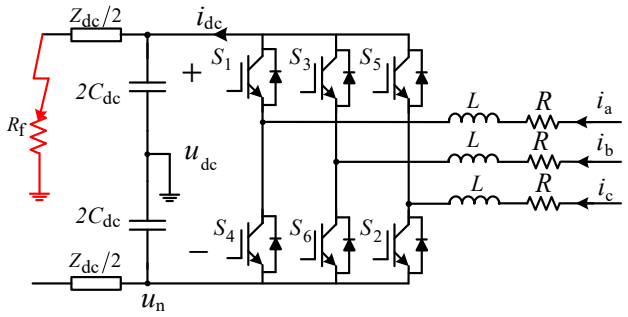

Figure 5. Positive cable ground fault of DC sub-grid.

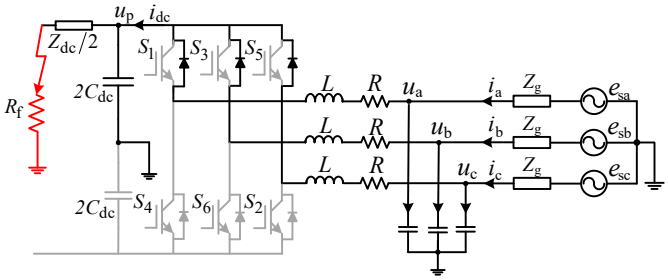

Figure 6. Single-pole ground-fault AC feed-in stage.

In the AC feedback stage, the anode of the lower bridge arm diode is connected to the negative pole of the DC sub-grid. The negative potential of DC sub-grid is $-u_{dc}$. This will result in the lower bridge arm diode being in an off state. The cathode potential of the upper bridge arm diode is close to 0, and the change in anode potential is consistent with the AC source, so its conductivity is closely related to the change in AC voltage value. It can be divided into six stages, as shown in Table 1 and Figure 7.

Table 1. Diode conduction at each stage.

Stage	Diode Conduction
I	D1, D5
II	D1
III	D1, D3
IV	D3
V	D3, D5
VI	D5

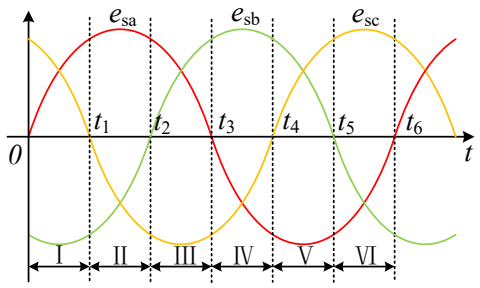

Figure 7. Segmented schematic.

For the fault situation of stage I, the short-circuit current path is shown in Figure 8. The short-circuit current i_{Da} of phase A can be expressed as

$$(L + L_{\mathrm{g}})\frac{\mathrm{d}i_{\mathrm{Da}}}{\mathrm{dt}} + (R + R_{\mathrm{g}})i_{\mathrm{Da}} = E_{\mathrm{sa}}\sin(\omega t + \alpha_{\mathrm{sa}}) - U_{\mathrm{p}}\sin(\omega t + \alpha_{\mathrm{p}}) \tag{3}$$

where α_{sa} and α_{p} are the initial phases of the voltage source of phase A and positive electrode capacitor voltage, respectively.

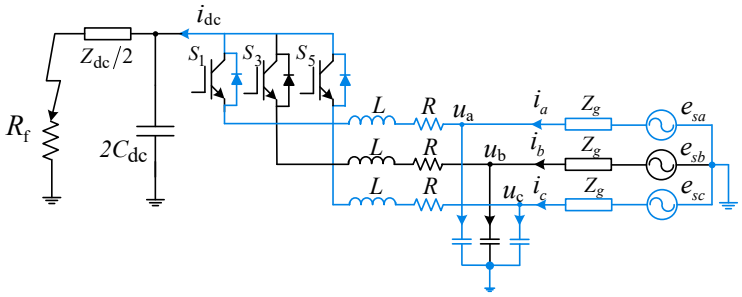

Figure 8. Diode conduction of each bridge arm in stage I.

The short-circuit current can be deconstructed into periodic $i_{p\mathrm{I}}$ and non-periodic $i_{\alpha\mathrm{I}}$ components by solving first-order, non-linear Equation (3):

$$i_{\mathrm{Da}} = i_{p\mathrm{I}} + i_{\alpha\mathrm{I}} \tag{4}$$

where the periodic components can be expressed as

$$i_{p\mathrm{I}} = \frac{\dot{E}_{\mathrm{sa}} - \dot{U}_{\mathrm{p}}}{j\omega L + R + Z_{\mathrm{g}}}. \tag{5}$$

The periodic component of the short-circuit current can be rewritten using the node voltage method, as follows:

$$\left(\frac{2}{j\omega L + R + Z_{\mathrm{s}}} + \frac{1}{Z_{\Sigma}^{\mathrm{dc}}}\right)\dot{U}_{\mathrm{p}} = \frac{\dot{E}_{\mathrm{sa}} + \dot{E}_{\mathrm{sc}}}{j\omega L + R + Z_g} \tag{6}$$

where Z_{Σ}^{dc} is the equivalent impedance of the internal resistance and voltage stabilizing capacitor in the DC sub-grid.

$$Z_{\Sigma}^{\mathrm{dc}} = (1/j2\omega C_{\mathrm{dc}})//(Z_{\mathrm{dc}}/2 + R_{\mathrm{f}}) \tag{7}$$

Due to the fact that the internal resistance of the DC sub-grid is much smaller than the equivalent impedance and the filter impedance of AC sub-grid, the term $\dot{E}_{\mathrm{sb}} = -(\dot{E}_{\mathrm{sa}} + \dot{E}_{\mathrm{sc}})$ can be ignored. At the same time, for the sake of simplicity in calculation, the initial phase

angle is set to 0. Therefore, the periodic component of the steady-state, short-circuit current can be approximated as

$$\begin{aligned} i_{pI} &= \frac{(2Z_{\Sigma}^{dc}+j\omega L+R+Z_g)\dot{E}_{sa}+Z_{dc}\dot{E}_{sb}}{(2Z_{\Sigma}^{dc}+j\omega L+R+Z_g)(j\omega L+R+Z_g)} \\ &\approx \frac{\dot{E}_{sa}}{j\omega L+R+Z_g} = I_m \sin(\omega t-\varphi) \end{aligned} . \tag{8}$$

At time t = 0, the current of phase A is $I_a(0)$, and the expression for the non-periodic component is

$$i_{\alpha I} = [I_a(0) - I_m \sin\varphi]e^{-t/T_a}. \tag{9}$$

The duration of stage I is approximately one-sixth of a cycle, which is 3.33 ms. Therefore, the fluctuation of non-periodic components is not significant in a short period of time, so it is approximated as the value at t = 0:

$$i_{\alpha I} = I_a(0) + I_m \sin\varphi. \tag{10}$$

The formula for the total current in stage I can be obtained from Equations (8) and (10):

$$i_{DaI} = I_a(0) + I_m \sin\varphi + I_m \sin(\omega t-\varphi). \tag{11}$$

During stages I to III, the voltage of phase A is positive, and the corresponding steady-state, short-circuit current is positive. In stages IV to VI, the voltage of phase A becomes negative, and the steady-state, short-circuit current is also negative, which can be replaced by $-I_m$. According to the above derivation process, the expression for the total current of phase A in stages II to VI is

$$\begin{cases} i_{DaII} = I_a(t_1) + I_m(\sin\varphi + \sin(\omega(t-t_1)-\varphi)) \\ i_{DaIII} = I_a(t_2) + I_m(\sin\varphi + \sin(\omega(t-t_2)-\varphi)) \\ i_{DaIV} = I_a(t_3) - I_m(\sin\varphi + \sin(\omega(t-t_3)-\varphi)) \\ i_{DaV} = I_a(t_4) - I_m(\sin\varphi + \sin(\omega(t-t_4)-\varphi)) \\ i_{DaVI} = I_a(t_5) - I_m(\sin\varphi + \sin(\omega(t-t_5)-\varphi)) \end{cases} . \tag{12}$$

In the formula, $I_a(t_k)$ is the instantaneous value of phase A current at time t_k and, when k = 1, 2, or 3, $I_a(t_k)$ can be expressed as

$$I_a(t_k) = I_a(0) + kI_m \sin\varphi + \sum_{n=1}^{n\le k} I_m \sin[\omega(t_n - t_{n-1})-\varphi]. \tag{13}$$

When k = 4 or 5, $I_a(t_k)$ can be expressed as:

$$I_a(t_k) = I_a(0) - (6-k)I_m \sin\varphi - \sum_{n=4}^{n\le k} I_m \sin[\omega(t_n - t_{n-1})-\varphi]. \tag{14}$$

The AC voltage source is a sine wave with a phase difference of 120°. According to the stage division in Figure 7, the duration of each stage is one-sixth of one cycle. Therefore, Equations (13) and (14) can be simplified as follows:

$$I_a(t_k) = I_a(0) + kI_m \sin\varphi + \sum_{n=1}^{n\le k} I_m \sin(\frac{\pi}{3}-\varphi), \tag{15}$$

$$I_a(t_k) = I_a(0) - (6-k)I_m \sin\varphi - \sum_{n=4}^{n\le k} I_m \sin(\frac{\pi}{3}-\varphi). \tag{16}$$

A new cycle will start from time t_6. The phase A voltage still corresponds to the variation process of stages I to VI. The expression for the fault current of the AC-sub-grid at this moment is

$$I_a(t_6) = I_a(t_5) + I_m \sin\varphi + I_m \sin\left(\frac{\pi}{3} - \varphi\right). \quad (17)$$

According to Equation (16), it can be deduced that

$$I_a(t_5) = I_a(0) - I_m \sin\varphi - I_m \sin\left(\frac{\pi}{3} - \varphi\right). \quad (18)$$

Substituting Equation (18) into Equation (17) yields

$$I_a(t_6) = I_a(0). \quad (19)$$

According to Equation (19), after six stages of variation, the value of the phase A current at the end of the cycle t_6 is exactly equal to the current value at the beginning of the cycle (t = 0); that is, the fault current of each cycle will cycle through the variation process of stages I to VI.

In summary, under the premise of a single-pole ground fault in the DC sub-grid and normal operation of the AC sub-grid, the BPC utilizes AC voltage changes to achieve energy conversion during the transient stage, and the conduction circuits corresponding to different voltage values are also different. By deducing expressions for the fault current in each stage, it can be seen that the initial current value of the $(n + 1)$th cycle is equal to the initial current value of the n-th cycle. The AC current lags behind the voltage and exhibits periodic changes. Furthermore, due to the unidirectional conduction characteristics of diodes, the AC current in each phase is positive.

3. Current Limitation Control Strategy for DC Fault Current

From the analysis of fault characteristics of the DC sub-grid in Section 2, it can be seen that the DC short-circuit current shows the characteristics of high numerical value and instantaneous rate of change, due to the small equivalent impedance in the DC sub-grid, which brings great challenges to the design and operation of DC circuit breaker. In addition, the DC fault identification speed is limited, and it is difficult to suppress the damage of the short-circuit current to the switching devices by only locking the converter. Moreover, the operating characteristics of AC/DC hybrid microgrid do not allow all converters to be locked at the same time. For DC short-circuit current protection, a control system for power converters can also be designed to enable hybrid microgrid systems to have the ability to limit fault currents.

When a fault occurs on the DC sub-grid, the power transmission direction is from the AC to the DC sub-grids. BPCs work in the rectification state. This paper introduces a virtual impedance control method to feed the stored energy of the DC capacitor into the AC sub-grid based on the constant DC voltage control method, which can reduce the growth amplitude and change rate of the DC fault current.

3.1. Principle of Current Limitation Control Strategy

The BPC operates in a rectification state, and usually adopts voltage and current dual-loop control. The function of the voltage control loop is to control the DC bus voltage, while the function of the current control loop is to control the current according to the reference value output by the voltage control loop. Figure 9 shows the equivalent circuit diagram of a hybrid microgrid system during an inter-pole, short-circuit fault, where R_{eq} is the virtual resistance, i_l is the DC current, and the physical meanings of the other parameters are the same as those in Section 2.

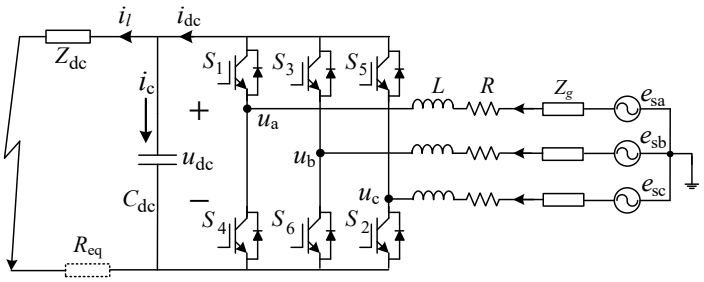

Figure 9. Equivalent circuit diagram of inter-pole, short-circuit fault.

For ease of calculation, the internal resistance Z_g of the AC power supply is ignored. According to Figure 9, without considering the virtual resistance, the power converter operates in a rectification state and the mathematical model in the dq coordinate system is

$$e_{sd} = L\frac{di_d}{dt} + Ri_d - \omega Li_q + u_d, \tag{20}$$

$$e_{sq} = L\frac{di_q}{dt} + Ri_q + \omega Li_d + u_q \tag{21}$$

where e_{sd} and e_{sq} are the d- and q-axis voltage values of the AC power supply, respectively.

Due to the coupling of the d- and q-axis variables in the above equation, an e_{sd} and e_{sq} feedforward decoupling control strategy is adopted. Under the action of the current loop regulator controlled by PI, the control equations of u_d and u_q are as follows:

$$u_d = -(k_{pi} + \frac{k_{ii}}{s})(i_{dref} - i_d) - \omega Li_q + e_{sd}, \tag{22}$$

$$u_q = -(k_{pi} + \frac{k_{ii}}{s})(i_{qref} - i_q) + \omega Li_d + e_{sq}. \tag{23}$$

Decoupling control of the current inner loop is achieved through Formulas (20)~(23), as shown in Figure 10.

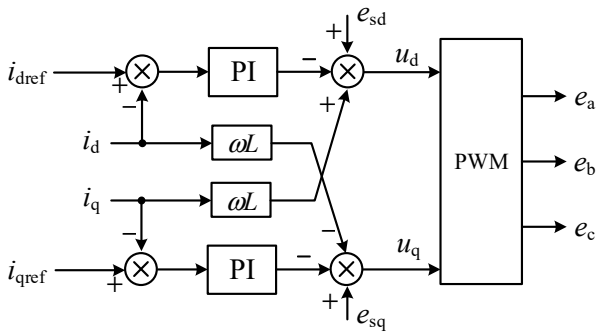

Figure 10. Current loop decoupling control block diagram.

It is assumed that the electromotive force vector e_{dq} of the power grid coincides with the d-axis in a two-phase rotating coordinate system, and the component e_q of the electromotive force vector on the q-axis is 0. Meanwhile, the current reference value given by the q-axis is usually 0 in voltage and current dual-loop control. Due to the symmetry of d-axis and q-axis current control, the design of a current regulator will be illustrated using d-axis current control as an example. Considering the small inertia characteristics of delay and PWM control in current signal sampling, the decoupled i_d control block diagram is shown in Figure 11.

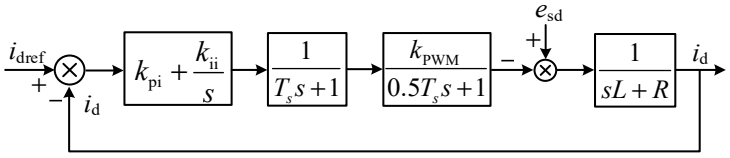

Figure 11. Diagram of d-axis current control loop.

The current control loop should have both good current following performance and anti-interference performance. However, when the anti-interference performance of the control system is enhanced, the following performance will decrease. To further improve the performance of control system, a composite control strategy that utilizes feedforward compensation to suppress disturbances can be adopted, as shown in Figure 12.

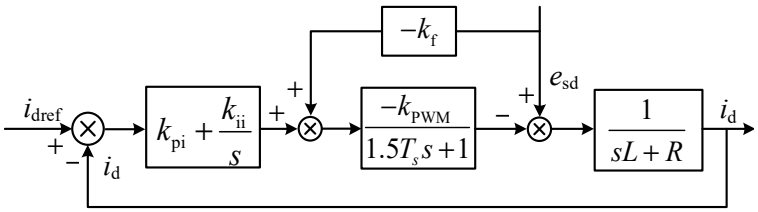

Figure 12. Diagram of composite current control loop.

In order to balance the following performance and anti-interference performance of the current control loop, the PI regulator is designed according to a typical Type I system, and the proportional and integral control parameters are calculated using the following formulas:

$$k_{pi} = \frac{R\tau_i}{3T_s k_{PWM}}, \tag{24}$$

$$k_{ii} = \frac{k_{ip}}{\tau_i} = \frac{R}{3T_s k_{PWM}} \tag{25}$$

where $\tau_i = L/R$.

The control purpose of the voltage control loop is to stabilize the DC capacitor voltage. To simplify control system design, when the switching frequency is much higher than the AC power supply frequency, only the low-frequency component of the switching function S_i (i = a, b, c) is considered, and the high-frequency harmonic component of PWM is ignored:

$$\begin{cases} S_a = 0.5 + 0.5m\cos(\omega t - \varphi) \\ S_b = 0.5 + 0.5m\cos(\omega t - \varphi - 120^\circ) \\ S_c = 0.5 + 0.5m\cos(\omega t + \varphi - 120^\circ) \end{cases} \tag{26}$$

where φ is the initial phase angle of the fundamental wave of the switching function, m is the duty cycle of PWM modulation, and $m = 1$ when the power transmission efficiency of the converter is at its maximum.

According to Figure 9, the KCL equation for DC capacitor nodes can be expressed as

$$C\frac{du_{dc}}{dt} = S_a i_a + S_b i_b + S_c i_c - i_l. \tag{27}$$

Setting $i_q = 0$ in the control process and applying the Clark transform to formula (27), the following can be obtained:

$$C\frac{du_{dc}}{dt} = \frac{3}{2}S_d i_d - i_l. \tag{28}$$

When deriving the control expression for the voltage loop, the maximum value of Sd is taken as 0.5 and the expression in the frequency domain is

$$sCU_{\mathrm{dc}} = \frac{3}{4} I_{\mathrm{d}}(s) - I_l(s). \tag{29}$$

Based on the above analysis, the voltage loop control structure diagram is shown in Figure 13, where $G_i(s)$ is the current loop transfer function.

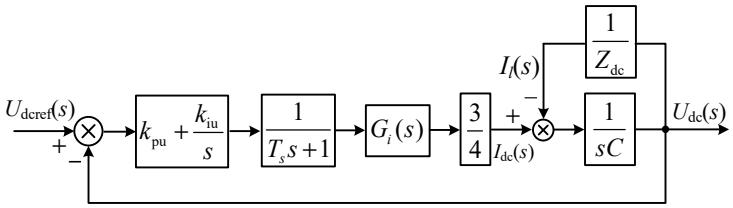

Figure 13. Diagram of voltage control loop.

In Figure 9, a virtual resistor connected in series with the original DC impedance is added to the DC sub-grid, and the DC capacitor voltage is represented as

$$U_{\mathrm{dc}}(s) = (R_{\mathrm{eq}} + Z_{\mathrm{dc}}) I_l(s). \tag{30}$$

The equivalent resistance value of the virtual resistor feedforward control is

$$R_{\mathrm{eq}} = \frac{\tau_{\mathrm{i}} s}{\tau_{\mathrm{f}} s + 1} i_l \tag{31}$$

where τ_{f} is the time constant of a low-pass filter, which is set at one-tenth of the switching frequency, and τ_{i} is the differential coefficient of i_{l}.

The normal and fault operation status of the DC sub-grid can be determined based on the instantaneous rate of current change, and the resistance value of the virtual resistor can be adjusted accordingly.

When the DC sub-grid is operating normally, R_{eq} approaches 0. When a DC fault occurs, the R_{eq} value increases to limit the short-circuit current. After the differential section, a limiting section for R_{eq} needs to be added to avoid excessive virtual resistance affecting the stable operation of the system. The overall control diagram of the virtual resistor is shown in Figure 14.

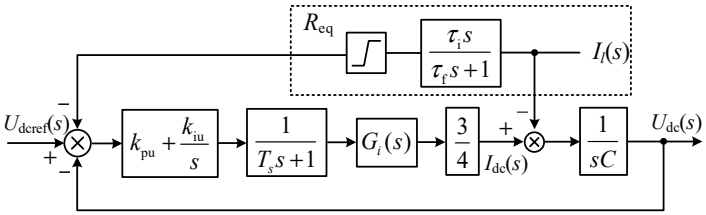

Figure 14. Control block diagram based on virtual resistance.

3.2. Virtual Resistor Parameter Design

The virtual resistance control strategy can adjust the resistance value according to the DC current change rate. However, when the R_{eq} value is too small, the effect of suppressing the short-circuit current cannot be significantly achieved. When the R_{eq} value is too large, the capacity requirement for the power converter is increased and the instantaneous response speed of the system will also slow down. From the perspective of power transmission, there is a relationship between R_{eq} and the output power of the converter. The maximum resistance value can be set as

$$R_{\mathrm{eq}} = \frac{P}{i_l^2} \left(\leq R_{\mathrm{eqmax}} = \frac{P_N}{i_{lN}^2} \right) \tag{32}$$

where P_N is the rated power and i_{lN} is the rated DC current.

When a DC sub-grid experiences an inter-pole, short-circuit or a single-pole ground fault, the transient process goes through the capacitor discharge stage without the consideration of virtual resistors. This process can be represented using a second-order differential equation:

$$L_{\mathrm{dc}} C_{\mathrm{dc}} \frac{\mathrm{d}u_{\mathrm{dc}}}{\mathrm{d}t^2} + R_{\mathrm{dc}} C_{\mathrm{dc}} \frac{\mathrm{d}u_{\mathrm{dc}}}{\mathrm{d}t} + u_{\mathrm{dc}} = 0 \tag{33}$$

where L_{dc} and R_{dc} are the total inductance and total resistance in the short-circuit circuit, respectively.

The initial value of the DC voltage at the moment before the fault is U_0 and the initial value of the DC current is I_0. The expression for the fault current is expressed as

$$i_l(t) = i_{\mathrm{dc}}(t) - i_C(t) = \frac{U_0}{\omega_1 L_{\mathrm{dc}}} e^{-\tau t} \sin(\omega_1 t) - \frac{I_0 \lambda_1}{\omega_1} e^{-\tau t} \sin(\omega_1 t - \varphi) \tag{34}$$

where $\tau = R_{\mathrm{dc}}/L_{\mathrm{dc}}$, $\lambda_1 = \sqrt{\tau^2 + \omega_1^2}$, $\omega_1 = \sqrt{1/(L_{\mathrm{dc}} C_{\mathrm{dc}}) - (R_{\mathrm{dc}}/L_{\mathrm{dc}})^2}$, and $\varphi = \arctan(\omega_1/\tau)$.

Inter-pole, short-circuit faults and single-pole ground faults are serious metal short-circuit faults. The resistance value in the faulty circuit is almost zero; therefore, Equation (34) can be simplified as

$$i_l(t) = \frac{U_0}{\sqrt{L_{\mathrm{dc}}/C_{\mathrm{dc}}}} \sin(\omega_1 t) - I_0 \sin(\omega_1 t - \frac{\pi}{2}). \tag{35}$$

After differential calculation, the change rate of the current $i_l(t)$ can be obtained as

$$\frac{\mathrm{d}i_l}{\mathrm{d}t} = \frac{U_0}{L_{\mathrm{dc}}} \cos(\omega_1 t) - \omega_1 I_0 \cos(\omega_1 t - \frac{\pi}{2}). \tag{36}$$

The initial stage of capacitor discharge can be approximated as

$$\frac{\mathrm{d}i_l}{\mathrm{d}t} \approx \frac{U_0}{L_{\mathrm{dc}}}. \tag{37}$$

In order to ensure that the interference generated by virtual resistors is minimal during normal system operation and as the virtual resistors have a significant current limiting effect when the system malfunctions, the differential coefficient of Equation (31) is set as

$$\tau_i = R_{\mathrm{eqmax}} / \frac{\mathrm{d}i_l}{\mathrm{d}t} = R_{\mathrm{eqmax}} / \frac{U_0}{L_{\mathrm{dc}}}. \tag{38}$$

U_0 is calculated by substituting the rated DC bus voltage value. When a fault occurs in the DC sub-grid, the change rate of the DC current is large and the virtual resistance value can reach its maximum value, Reqmax. The energy in the DC capacitor is fed into the AC sub-grid through a power converter. When there is a small disturbance in the DC sub-grid during normal operation of the system, the change rate is also relatively small, compared to when there is a fault, which ensures that the interference caused by the virtual resistance is relatively small.

4. Simulation Analysis

To verify the accuracy of the analysis of interaction effects of DC sub-net grid faults and the effectiveness of the fault suppression strategies mentioned above, hardware for use with the loop real-time simulation platform was built based on the RTDS (RTDS Technologies Inc., Winnipeg, MB, Canada) platform. The bidirectional power converter can be connected

to the Novacor host through analog output cards and digital input cards. The main wiring diagram is shown in Figure 15, and the structure of the AC and DC hybrid microgrid is shown in Figure 1. The model parameters are provided in Table 2.

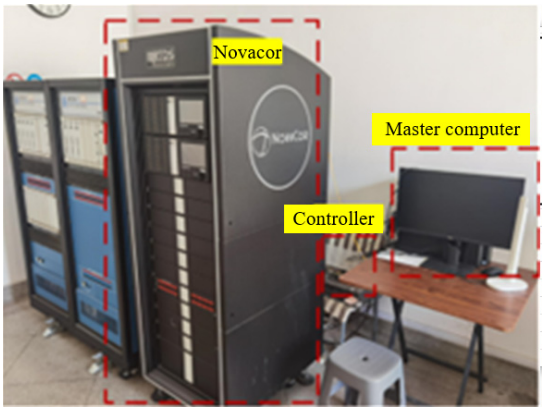

Figure 15. Test setup based on RTDS platform.

Table 2. Simulation model parameters.

Parameters	Value
DC voltage e_{dc}	600 V
AC voltage e_s	220 V, 50 Hz
Equivalent impedance of DC sub-grid Z_{dc}	0.1 Ω, 0.12 mH
DC stabilized capacitor C_{dc}	470 μF
Filter L, R, C	2 mH, 1×10^{-6} Ω, 300 μF
Equivalent impedance of AC sub-grid Z_g	0.75 Ω, 4.8 mH
Current inner loop control parameters k_{pi}, k_{ri}	39.87, 10.05
Voltage outer loop control parameters k_{pu}, k_{ru}	1.1, 20
Virtual resistance maximum value R_{eqmax}	12 Ω

When the DC sub-grid operates in a fault state with a DC bus voltage of 600 V and the AC sub-grid operates normally; the bidirectional power converter operates in a rectification state. Figure 16 shows the waveform of AC current response when an inter-pole, short-circuit fault occurs in the DC sub-grid. During the stage of simultaneous conduction of the diodes, the AC sub-grid is equivalent to a three-phase, short-circuit fault and the AC current rapidly increases to a three-phase, short-circuit current. As the non-periodic components of the current decay, the three-phase current exhibits a sinusoidal symmetric waveform in a steady state. The calculated and simulated current amplitudes under steady-state conditions are 67.24 A and 65.5 A, respectively, with an error of 2.66%, which generally conforms to the current expression in Equation (25).

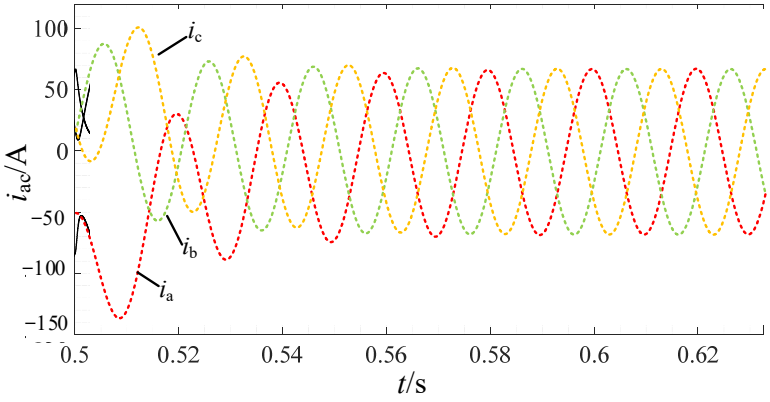

Figure 16. AC current waveform of inter-pole, short-circuit fault.

The waveform of phase A fault current when a single-pole ground fault occurs in the DC sub-grid is shown in Figure 17. Based on the analysis in Section 2 of this paper, the diodes work in an uncontrolled rectification state, and the AC short-circuit current changes unidirectionally during the AC feeding stage. The peak fault current in the calculation result is 76.1 A; slightly higher than the simulation result of 73.06 A, with an error of 4.11%.

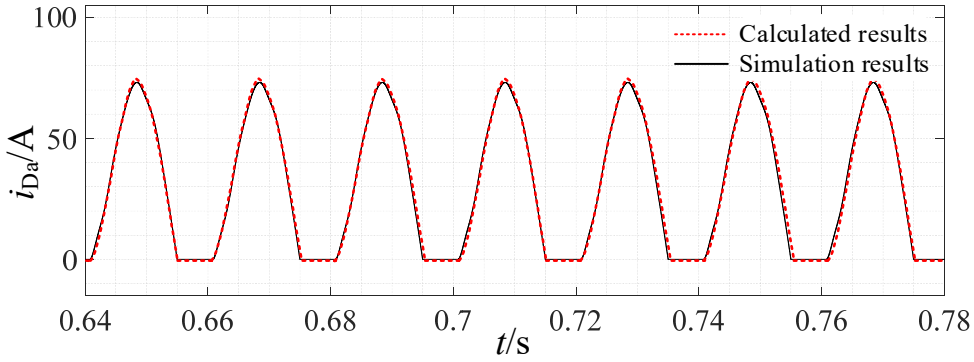

Figure 17. AC current waveform of single-pole ground fault.

In the theoretical analysis process, the influence of internal resistance Z_{dc} on the DC sub-grid is not considered. When considering its impact on short-circuit current, the growth rate of the short-circuit current will be slower than the decay rate. The current expression in Equation (17) can be modified to

$$I_a(t_6) = I_a(t_5) + I'_m \sin\varphi + I'_m \sin\left(\frac{\pi}{3} - \varphi\right) \tag{39}$$

where $I'_m < I_m$. The fault current in stage VI will decay to 0 and, due to the unidirectional conduction characteristic of the diode, the current will remain at 0 until the next cycle repeats the change process of six stages again. Figure 18 shows the corresponding relationship between AC voltage phase B and the fault current in stages I–VI. From the graph, it can be seen that 0.664 s is the start time of the cycle, and each stage takes 3.33 ms. The fault current value in stage I is 0, which is due to the impedance characteristics in the circuit. The measured fault current response lags behind the AC voltage by 3.63 ms.

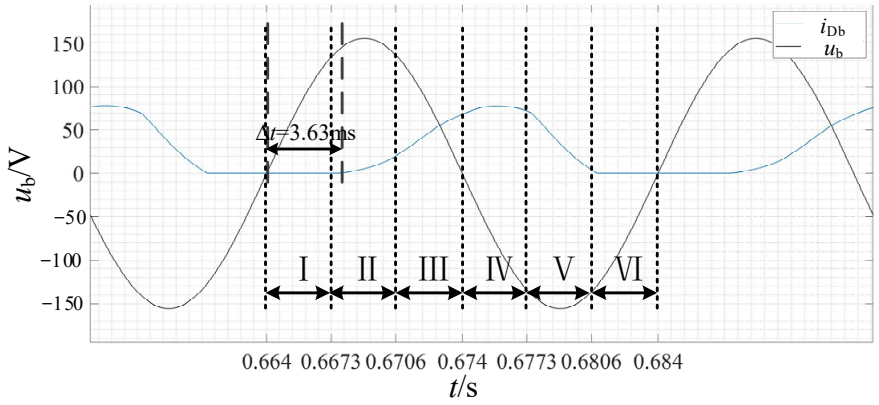

Figure 18. Corresponding relationship between AC voltage and fault current in stages I–VI of phase B.

The calculation formula for hysteresis angle is expressed as

$$\varphi = \arctan\frac{\omega(L_{dc} + L + L_g)}{R_{dc} + R + R_g} \tag{40}$$

Substituting the relevant parameters in Table 2 into Equation (40), the lag angle of the AC current is obtained, while the lag time measured using the oscilloscope was converted into an angle of 65.3°. This basically verifies the correspondence between the simulation results and theoretical calculations.

Figure 19 compares the current waveforms of the freewheeling diode for inter-pole, short-circuit faults and single-pole ground faults. The transient processes of both types of faults in the DC sub-grid passed through the capacitor discharge stage and the AC feedback stage. However, the diode current of inter-pole, short-circuit faults shows a sharp overcurrent phenomenon, compared to that of a single-pole ground fault, which is about three times that under normal operations. The difference lies in the capacitor discharge stage, where the capacitor voltage under both types of faults meets the condition of oscillation and zero crossing due to the system's underdamping state. However, in the case of a single-pole ground fault, there is AC sub-grid support, and the voltage of the non-fault pole can maintain Udc but not zero. Therefore, it will not enter the third stage, similar to the simultaneous conduction of diodes, and the AC current will not reach the value of the three-phase, short-circuit current.

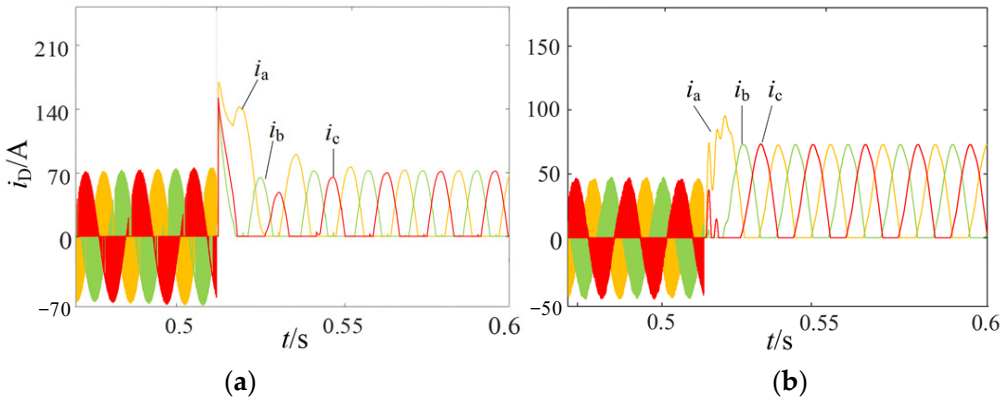

Figure 19. Current waveform of freewheeling diode. (**a**) Inter-pole, short-circuit fault. (**b**) Single-pole ground fault.

To verify the impact of virtual impedance control on the normal operation of the system, a comparison was made among the waveform changes of the AC three-phase current, DC voltage, and DC current without current limitation control and with current limitation control.

According to Figure 20, it can be seen that, when the system is operating normally and no current limitation control strategy is added, the amplitude of the AC current is 73.5 A. After adding a current limitation control strategy, the amplitude of the AC current is 70.2 A. Thus, the current change rate is 4.76%. The data show that the current limitation control strategy slightly weakens the AC current response.

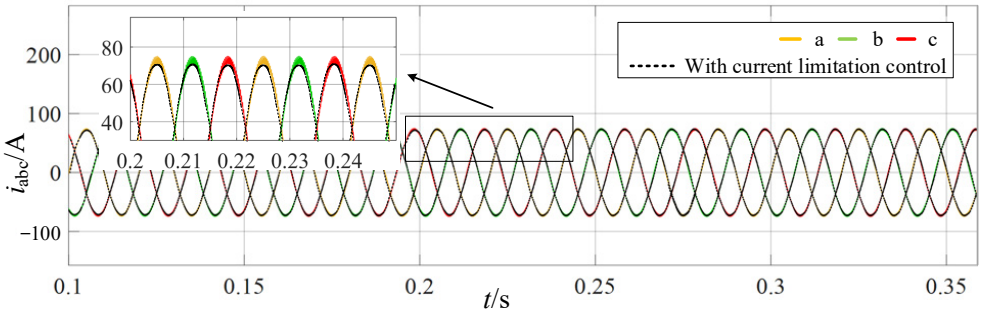

Figure 20. Comparison diagram of AC current with and without current limitation control strategy.

According to the DC current waveforms in Figure 21, the peak and steady-state values of current variation without the current limitation control strategy are 95.2 A and 50.7 A, respectively; meanwhile, when adding a current limitation control strategy, the peak and steady-state values of the current are 80 A and 50 A, respectively. It can be seen that current-limiting control also weakens the response effect of the DC current, but it has a suppressive effect on the initial current overshoot during operation of the system.

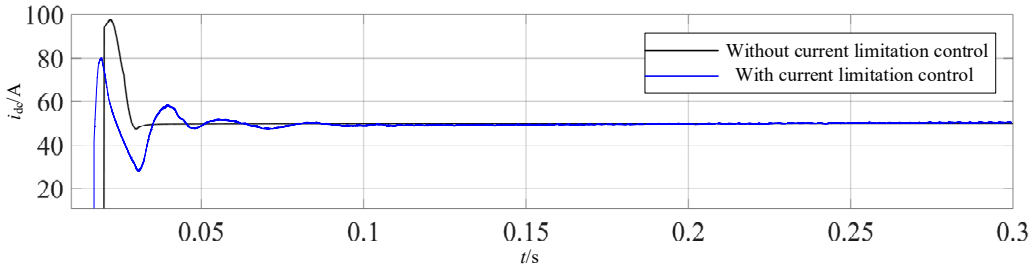

Figure 21. Comparison diagram of DC current with and without current limitation control strategy.

According to the DC voltage comparison chart shown in Figure 22, the overshoot and steady-state values of DC voltage without current limitation control are 610 V and 600 V, respectively. After adding the current limitation control strategy, these two values are 648 V and 600 V, respectively. It can be seen that current limitation control has a certain degree of impact on the voltage response during the initial operation of the system. After the system reaches a steady state, the steady-state values of each electrical quantity are generally the same.

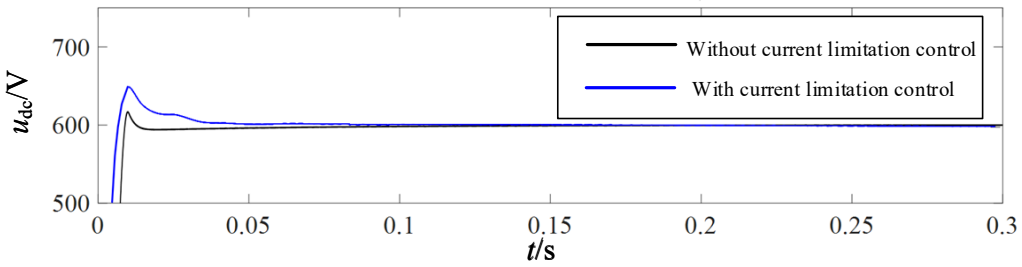

Figure 22. Comparison diagram of DC voltage with and without current limitation control strategy.

The inter-pole, short-circuit fault of the DC sub-grid occurs 0.4 s after the system reaches a stable operating state. Figures 23–25 show waveforms of AC three-phase current, DC current, and DC voltage with and without current limitation control under the fault.

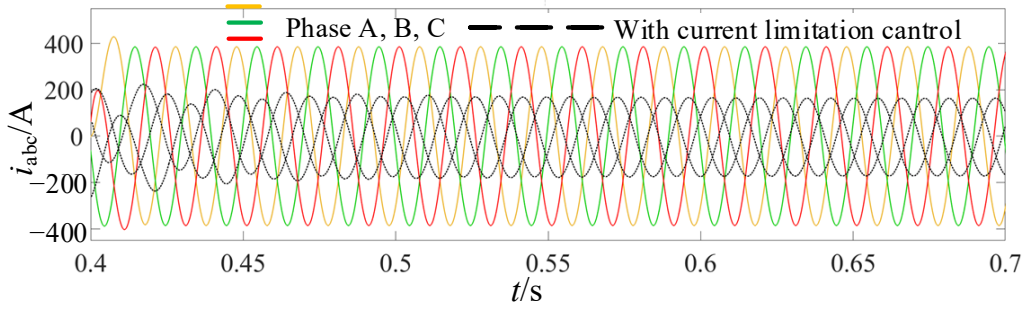

Figure 23. Three-phase current waveform with and without current limitation control under fault operation.

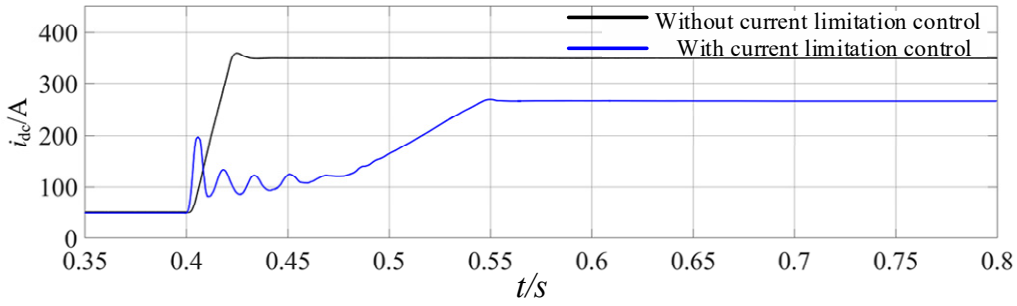

Figure 24. DC current waveform with and without current limitation control under fault operation.

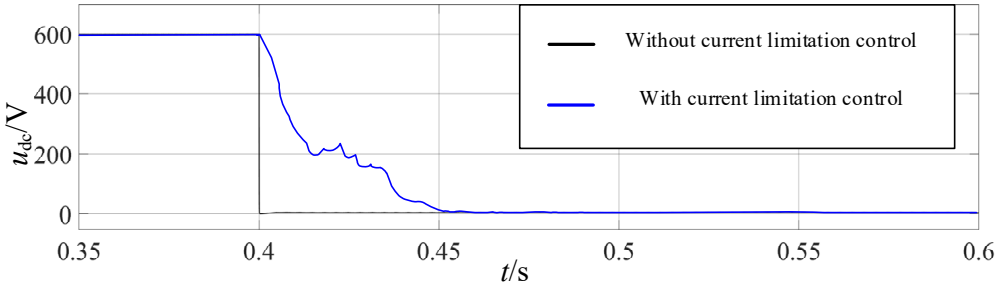

Figure 25. DC voltage waveform with and without current limitation control under fault operation.

It can be seen, from Figure 23, that the peak value of three-phase AC current without current limitation control increased from 73.5 A to 387 A after the occurrence of an inter-pole, short-circuit fault, while the fault current amplitude after adding current limitation control is 182 A. According to analysis of the transient process of inter-pole, short-circuit faults in the previous text, it is equivalent to a three-phase, short-circuit fault occurring in the AC sub-grid during the stage of simultaneous conduction of diodes. The denominator of the expression for AC current calculation includes DC resistance. The decrease in the amplitude of the AC current indicates that the virtual impedance current limitation control begins to take effect as the change rate of the DC fault current increases. The DC current limitation control strategy also alleviates the problem of AC overcurrent, to a certain extent.

Figure 24 shows the current waveform under the fault state of the DC sub-grid. In the figure, the black lines represent the current curve without current limitation control, while the blue lines represent the current curve with current limit control. It can be seen, from the graph, that when current limitation control is introduced, the duration of the fluctuation of DC current lasts for 0.05 s after the fault occurs and then continues to increase to the steady-state value of 260 A. When there is no current limitation control, the duration of fluctuation after the DC fault occurs lasts for 0.018 s and rapidly increases to a steady-state value of 345 A. Thus, the virtual-impedance-based, current-limiting control strategy proposed in this paper can reduce the DC short-circuit current from 345 A to 260 A under fault conditions, and its transient impact is also alleviated. In contrast, Figure 25 shows the voltage waveform under the fault state of the DC sub-grid, and the meaning of lines is the same as in Figure 24. Similarly, the DC voltage drops linearly from a steady-state value of 600 V to 0 V at the time of fault occurrence without current limitation control added. After adding current limitation control, the time for the DC voltage to decrease from 600 V to 0 V is extended to 0.05 s. The current limitation control strategy can reduce the change rate of the fault current from 19.1 kA/s to 2.73 kA/s. In summary, employment of the proposed current limitation control strategy can effectively reduce the impact of fault currents and reduce the impact of transient voltage drops, greatly protecting key equipment in the microgrid from the impact of faults.

Figure 26 shows the variation in the d-axis current with and without current limitation control. After the fault occurred, the d-axis current rapidly increased under the traditional, consistent DC voltage dual-loop control, and the direction of energy transmission remained

consistent with that before the fault occurred. The energy stored in the capacitor also discharges towards the fault point, which causes a short-term overshoot of 0.418 s. After adding current limitation control, the i_d changes in the opposite direction and the stable value is opposite to the sign when no fault occurs. The addition of the current limitation strategy reduces the discharge of capacitors towards the fault location and then feeds energy to the AC sub-grid, which will limit the growth of the fault current.

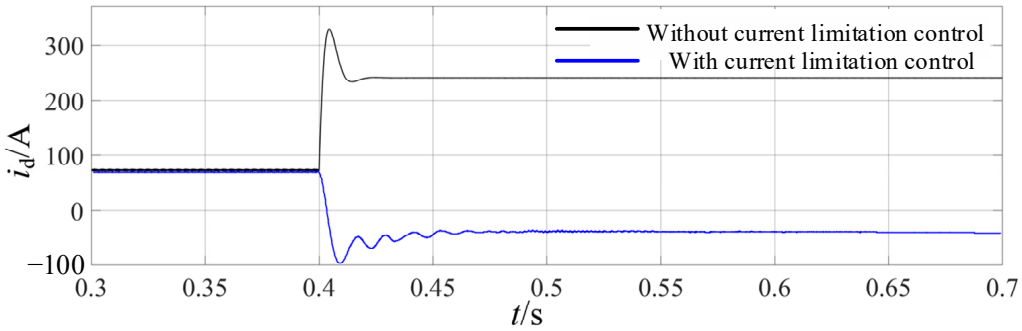

Figure 26. Current inner loop, d-axis, current-control waveform.

5. Conclusions

This study investigated the DC fault propagation mechanism and proposed a current limitation control strategy. The analyzed mechanism and fault suppression strategy were then simulated and verified based on the RTDS hardware using a loop real-time simulation platform. The summary is as follows.

This paper used inter-pole, short-circuit faults and single-pole ground faults in the DC sub-grid as examples to analyze the transient changes in the fault circuit and derive the expressions of AC short-circuit currents affected by DC faults. The expression of the AC current under an inter-pole, short-circuit fault in the DC sub-grid was similar to that of a three-phase, short-circuit fault current in the AC sub-grid, while the AC short-circuit current under the single-pole ground fault lagged behind the AC power supply and exhibited the characteristics of periodic variation. Meanwhile, the error between the calculated short-circuit current expression derived from theory and the simulation results did not exceed 5%. In addition, the fault current under inter-pole, short-circuit faults increases more rapidly and has a larger amplitude, compared to that for single-pole ground faults, which are more likely to cause equipment damage.

This paper proposed a current limitation control strategy to address the rapid increase in current caused by DC faults. On the basis of constant DC voltage control in AC/DC hybrid microgrids, a virtual impedance control link was added. The proposed control strategy only needs to activate the control based on the change rate of the DC current, without additional fault detection systems. During normal operations, virtual impedance has a relatively small impact on the steady-state characteristics of the system. In the case of a fault, the virtual impedance resistance value is automatically adjusted to limit the change rate and amplitude of the fault current. Through simulation verification, the proposed current limitation control was found to not affect the normal operation of the system and could effectively slow down the current change rate and amplitude in the event of a DC fault. Under the framework of the DC fault current limitation control strategy, the increase in the fault current decreased and its change rate decreased from 19.1 kA/s to 2.73 kA/s.

A PI controller was adopted for the control framework in this paper. However, PI controllers operate on the control error of the previous moment and do not predict future control errors, which limits their control performance. In addition, it is difficult to simultaneously meet the requirements of overshoot and response time under the PI control architecture. Therefore, in subsequent research, the focus will be on predictive control algorithms based on virtual impedance and active disturbance rejection control algorithms, which can simultaneously meet the requirements of response time and overshoot.

Author Contributions: C.X.: methodology, software, validation, investigation, data curation, writing—original draft preparation; Y.R.: writing—review and editing, project administration, software; Q.C.: writing—review and editing, data curation; R.C.: writing—review and editing, software; L.W.: writing—original draft preparation, writing—review and editing. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by science and technology project of the STATE GRID Shanxi Electric Power Company (Analysis of the Impact Mechanism and Accuracy Improvement of Electric Energy Measurement for New Type Power Systems), grant number 52051L230002.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: Author Ruifen Cheng was employed by the State Grid Taiyuan Electric Power Supply Company. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest. The State Grid Taiyuan Electric Power Supply Company had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

References

1. Zhang, B.; Han, X.; Ren, C.; Zhang, D.; Wang, L.; Song, T. Circulating Current Suppression Method with Adaptive Virtual Impedance for Multi-bidirectional Power Converters Under Unbalanced Conditions. *CSEE J. Power Energy Syst.* **2023**, *9*, 77–87.
2. Zhang, B.; Han, X.; Meng, R.; Ren, C.; Wang, L.; Song, T.; Liu, Y. Adaptive virtual impedance control based on second-order generalized integral for circulating current suppression. *J. Power Electron.* **2021**, *21*, 13–26. [CrossRef]
3. Liang, Z.; Dong, Z.; Li, C.; Wu, C.; Chen, H. A Data-Driven Convex Model for Hybrid Microgrid Operation with Bidirectional Converters. *IEEE Trans. Smart Grid* **2023**, *14*, 1313–1316. [CrossRef]
4. Zhang, K.; Su, M.; Liu, Z.; Han, H.; Zhang, X.; Wang, P. A Distributed Coordination Control for Islanded Hybrid AC/DC Microgrid. *IEEE Syst. J.* **2023**, *17*, 1819–1830. [CrossRef]
5. He, L.; Li, Y.; Chu, X.; Shuai, Z.; Peng, Y.; Shen, Z.J. Single-Phase to Ground Fault Line Identification for Medium Voltage Islanded Microgrids with Neutral Ineffectively Grounded Modes. *IEEE Trans. Smart Grid* **2022**, *13*, 4312–4326. [CrossRef]
6. Ali, Z.; Terriche, Y.; Abbas, S.Z.; Hassan, M.A.; Sadiq, M.; Su, C.L.; Guerrero, J.M. Fault Management in DC Microgrids: A Review of Challenges, Countermeasures, and Future Research Trends. *IEEE Access* **2021**, *9*, 128032–128054. [CrossRef]
7. Vafamand, N.; Arefi, M.M.; Asemani, M.H.; Javadi, M.S.; Wang, F.; Catalão, J.P. Dual-EKF-Based Fault-Tolerant Predictive Control of Nonlinear DC Microgrids With Actuator and Sensor Faults. *IEEE Trans. Ind. Appl.* **2022**, *58*, 5438–5446. [CrossRef]
8. Du, K.J.; Ma, X.P.; Zheng, Z.X.; Li, C.S.; Hu, W.X.; Dong, K.S. LVRT Capability Improvement of DFIG-Based Wind Turbines with a Modified Bridge-Resistive-Type SFCL. *IEEE Trans. Appl. Supercond.* **2022**, *31*, 5603005. [CrossRef]
9. Sharma, S.; Tripathy, M. Differential Reactor Voltage Based Fault Detection and Classification for Smart DC Microgrid. *IEEE Trans. Ind. Inform.* **2023**, *19*, 11730–11741. [CrossRef]
10. Nougain, V.; Panigrahi, B.K. Detection of DC System Faults Based on the Principle of Threshold Violation in i-r Plane. *IEEE Syst. J.* **2021**, *15*, 856–864. [CrossRef]
11. De La Cruz, J.; Wu, Y.; Candelo-Becerra, J.E.; Vásquez, J.C.; Guerrero, J.M. Review of Networked Microgrid Protection: Architectures, Challenges, Solutions, and Future Trends. *CSEE J. Power Energy Syst.* **2024**, *10*, 448–467.
12. Yu, X.; Xiao, L. A DC Fault Protection Scheme for MMC-HVDC Grids Using New Directional Criterion. *IEEE Trans. Power Deliv.* **2021**, *36*, 441–451. [CrossRef]
13. Zheng, Z.; Zou, Y.; Xie, Q.; Liu, L.; Ren, J.; Xiao, X.; Zhang, J. Side Effect of VSC-HVDC on Commutation Failure in LCC-HVDC Caused by Sending End AC Faults. *IEEE Trans. Power Deliv.* **2024**, *39*, 1310–1313. [CrossRef]
14. Li, B.; Liao, K.; Yang, J.; He, Z. Transient Fault Analysis Method for VSC-Based DC Distribution Networks with Multi-DGs. *IEEE Trans. Ind. Inform.* **2022**, *18*, 7628–7638. [CrossRef]
15. Miao, X.; Zhao, D.; Lin, B.; Jiang, H.; Chen, J. A Differential Protection Scheme Based on Improved DTW Algorithm for Distribution Networks with Highly-Penetrated Distributed Generation. *IEEE Access* **2023**, *11*, 40399–40411. [CrossRef]
16. Gupta, A.; Pachar, R.K.; Mahela, O.P.; Khan, B. Fusion of Signal Processing Techniques to Design Current and Voltage Features Based Protection Scheme for Utility Grid with Renewable Energy Penetration. *IEEE Access* **2022**, *10*, 118222–118235. [CrossRef]
17. Li, Y.; Wang, Z.; Yang, J.; Wang, X.; Feng, J. Dynamic Equivalence Modeling for Microgrid Cluster by Using Physical-Data-Driven Method. *IEEE Trans. Appl. Supercond.* **2021**, *31*, 5401004. [CrossRef]
18. Naghizadeh, M.; Hojabri, H.; Muljadi, E. A Common-Grounded Single-Phase AC/Bipolar DC Hybrid Microgrid with a Four-Leg Interlinking Converter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2023**, *11*, 5337–5353. [CrossRef]
19. Behzadirafi, S.; De Leon, F. Closed-Form Determination of the Impedance Locus Plot of Fault Current Limiters: Asymmetrical Faults. *IEEE Trans. Power Deliv.* **2020**, *35*, 754–762. [CrossRef]

20. Islam, M.R.; Hasan, J.; Shipon, M.R.R.; Said, M.A.H.; Abuhussein, A.; Roy, T.K. Neuro Fuzzy Logic Controlled Parallel Resonance Type Fault Current Limiter to Improve the Fault Ride Through Capability of DFIG Based Wind Farm. *IEEE Access* **2020**, *8*, 115314–115334. [CrossRef]
21. Ghavidel, P.; Farhadi, M.; Dabbaghjamanesh, M.; Jolfaei, A.; Sabahi, M. Fault Current Limiter Dynamic Voltage Restorer (FCL-DVR) With Reduced Number of Components. *IEEE J. Emerg. Sel. Top. Ind. Electron.* **2021**, *2*, 526–534. [CrossRef]
22. So, J.; Lee, S.; Park, S.Y.; Choi, H.S.; Choi, K.; Kim, W.S. HTS FCL Module with Voltage of 500 V for DC Circuit Breaker. *IEEE Trans. Appl. Supercond.* **2021**, *31*, 5601504. [CrossRef]
23. Li, B.; He, J.; Li, Y.; Wen, W.; Li, B. A Novel Current-Commutation-Based FCL for the Flexible DC Grid. *IEEE Trans. Power Electron.* **2020**, *35*, 591–606. [CrossRef]
24. Zhou, H.; Yuan, J.; Sun, P.; Ye, C.; Liu, J.; Zheng, Y.; Cai, J. Bidirectional Hybrid X Shape FCL in HVdc System with Multifunctional Feature. *IEEE Trans. Power Electron.* **2023**, *38*, 5979–5993. [CrossRef]
25. Alasali, F.; Saidi, A.S.; El-Naily, N.; Alnaser, S.W.; Holderbaum, W.; Saad, S.M.; Gamaleldin, M. Advanced Coordination Method for Overcurrent Protection Relays Using New Hybrid and Dynamic Tripping Characteristics for Microgrid. *IEEE Access* **2022**, *10*, 127377–127396. [CrossRef]
26. Naghizadeh, M.; Gohari, H.S.; Hojabri, H.; Muljadi, E. New Single–Phase Three-Wire Interlinking Converter and Hybrid AC/LVDC Microgrid. *IEEE Trans. Power Electron.* **2023**, *38*, 4451–4463. [CrossRef]
27. Wang, R.; Liao, M.; Duan, X.; Xie, D.; Feng, Z.; Han, X. Research on the Arc Characteristics of a New Self-Driving Fault Current Limiter. *IEEE Trans. Plasma Sci.* **2024**, *52*, 126–133. [CrossRef]
28. Bhargav, R.; Gupta, C.P.; Bhalja, B.R. Unified Impedance-Based Relaying Scheme for the Protection of Hybrid AC/DC Microgrid. *IEEE Trans. Smart Grid* **2022**, *13*, 913–927. [CrossRef]